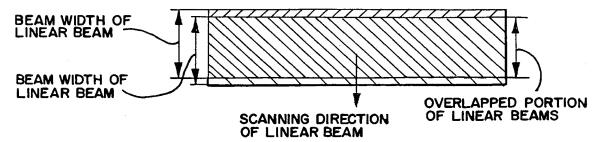
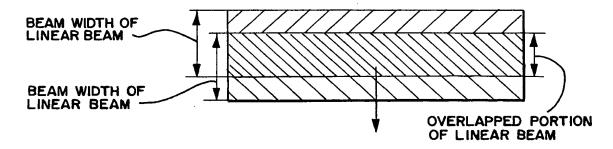




### FIG. 2A



#### FIG. 2B



#### FIG. 2C

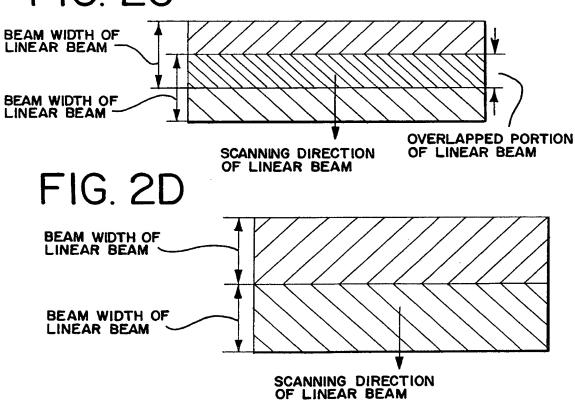
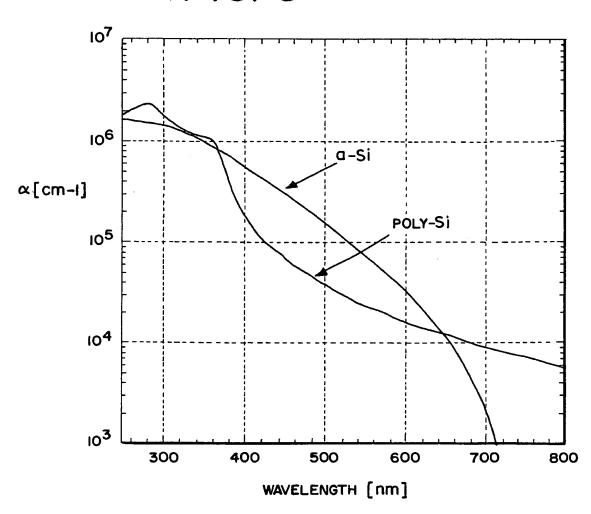
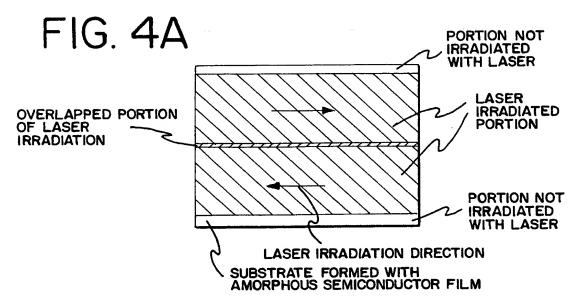
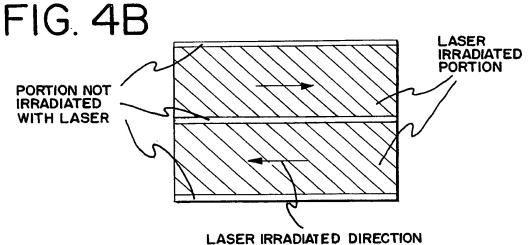
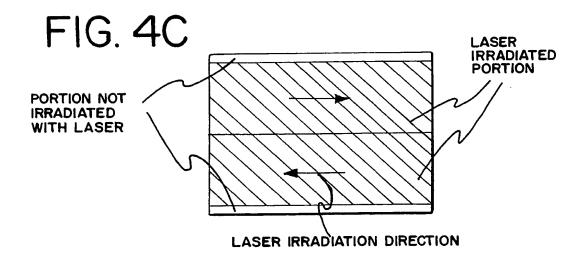


FIG. 3









# FIG. 5A

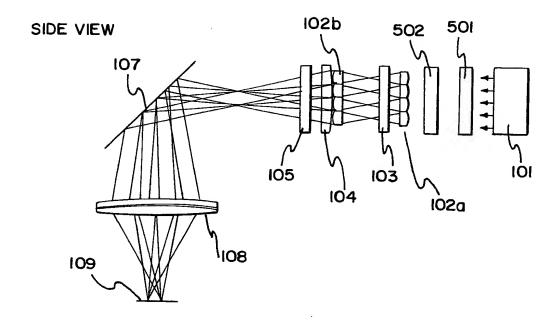
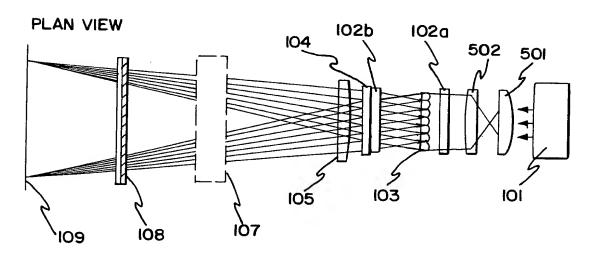


FIG. 5B



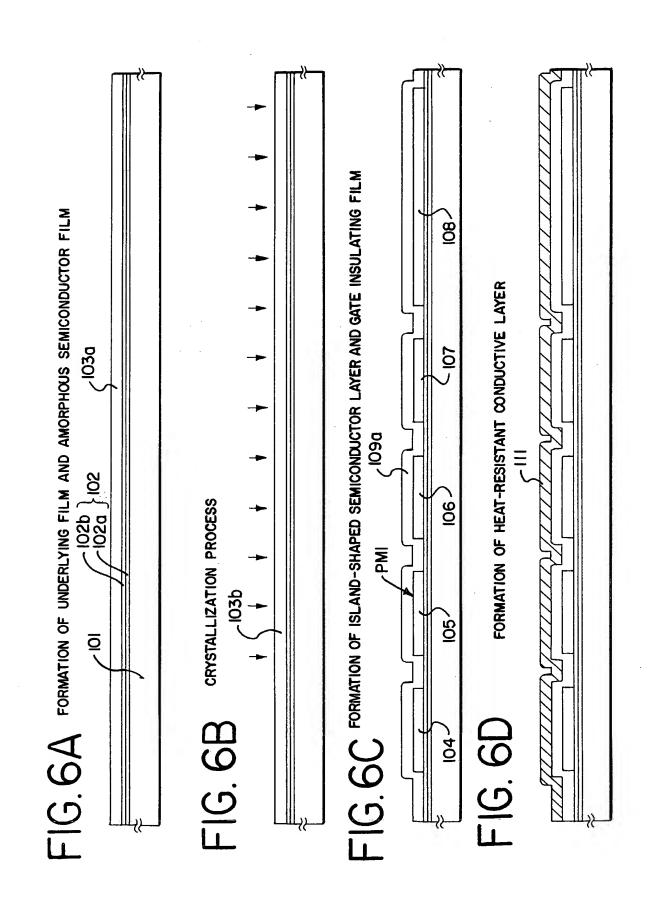


FIG. 7A FIRST ETCHING PROCESS/FIRST DOPING PROCESS (n+)

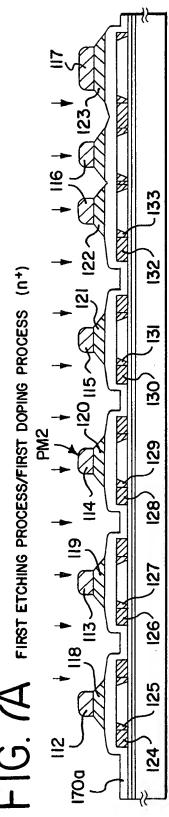


FIG. 7B SECOND ETCHING PROCESS/SECOND DOPING PROCESS (n-)

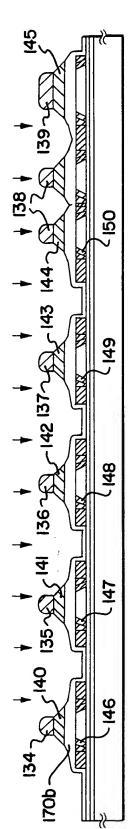


FIG. 7C P+ DOPING PROCESS

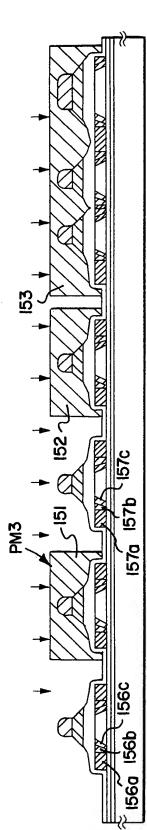
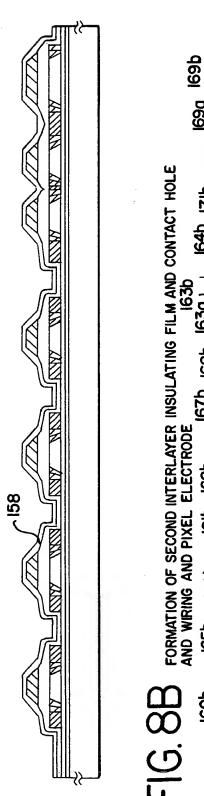
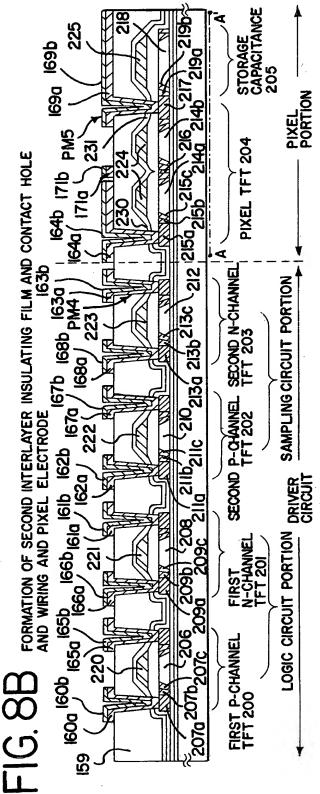
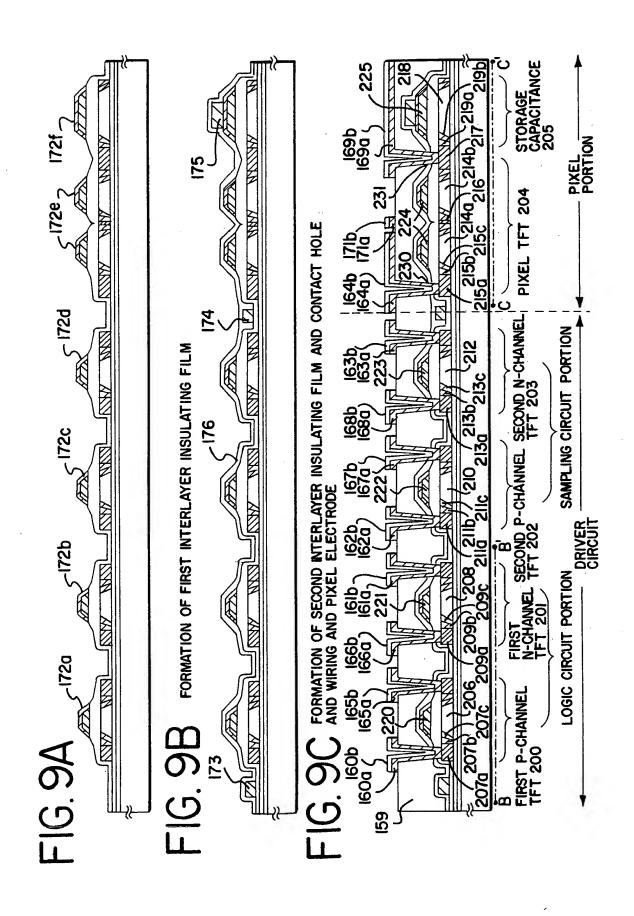


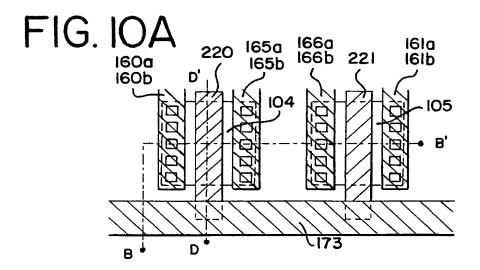
FIG. 8A

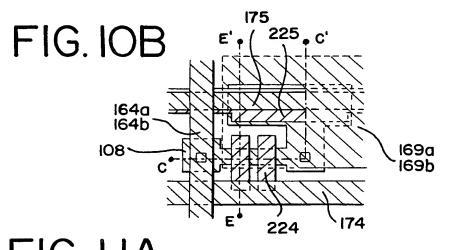
FORMATION OF FIRST INTERLAYER INSULATING FILM

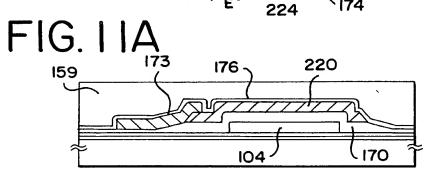


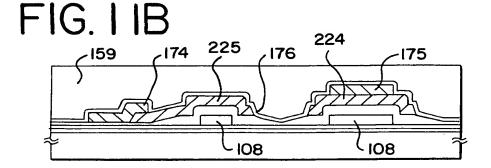




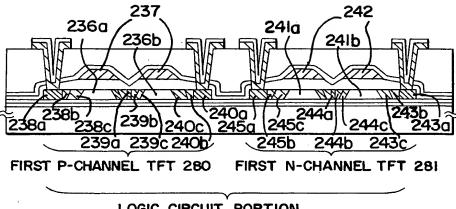






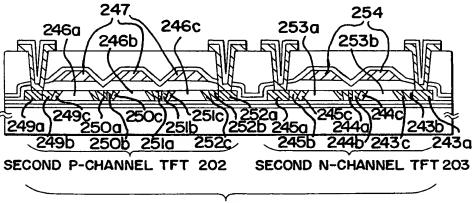


## FIG. 12A



LOGIC CIRCUIT PORTION

## FIG. 12B



SAMPLING CIRCUIT PORTION

## FIG. 13A

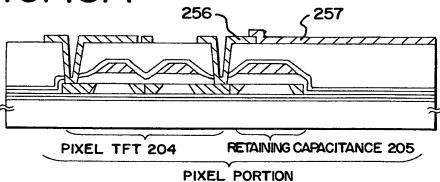
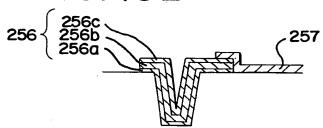


FIG. 13B



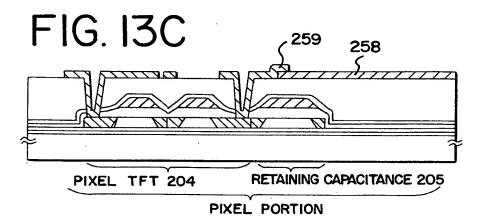


FIG. I3D

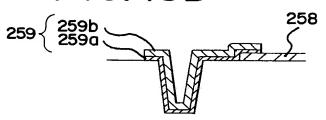
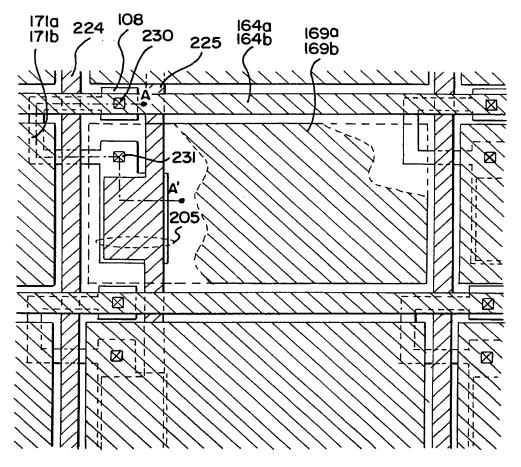


FIG. 14



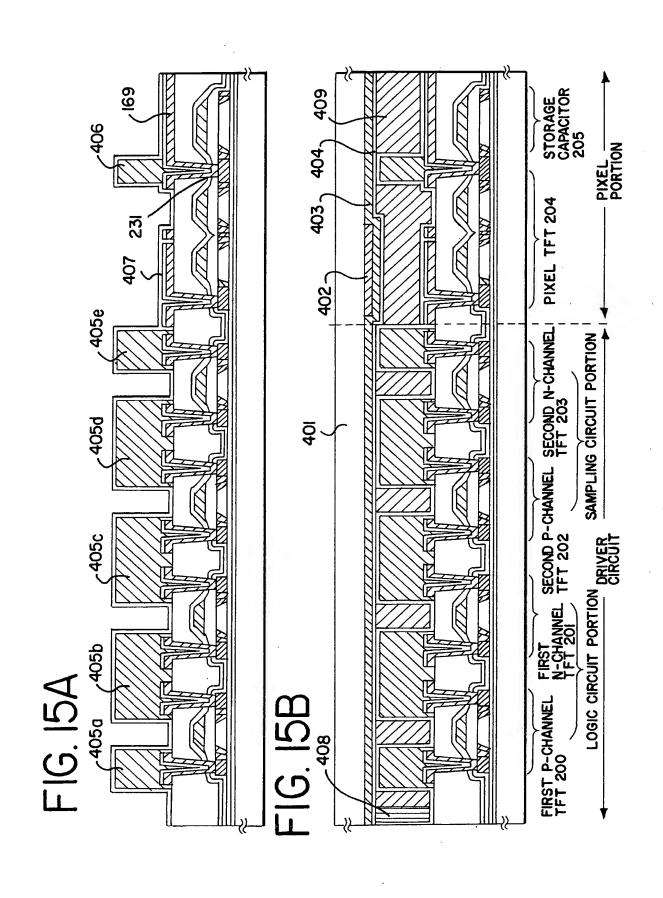


FIG. 16

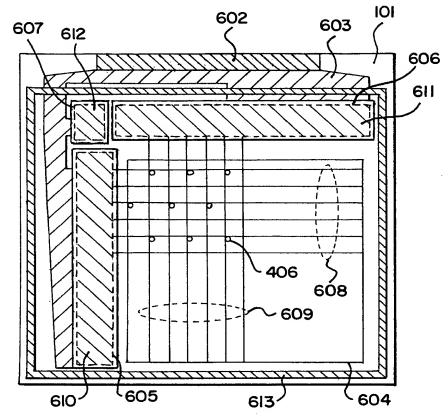
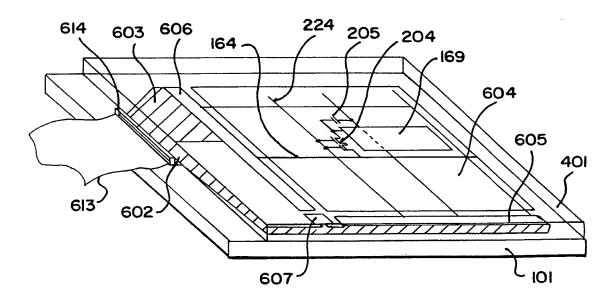
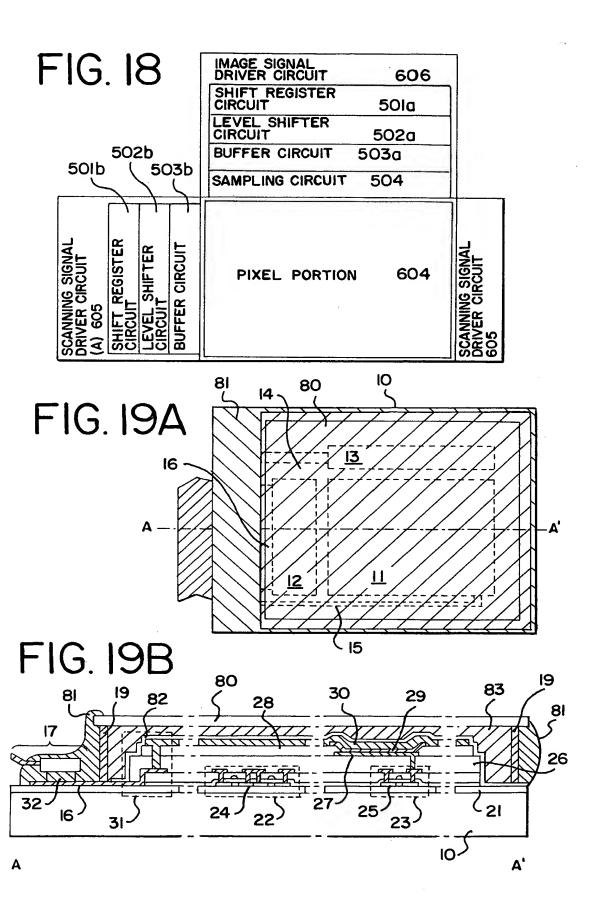
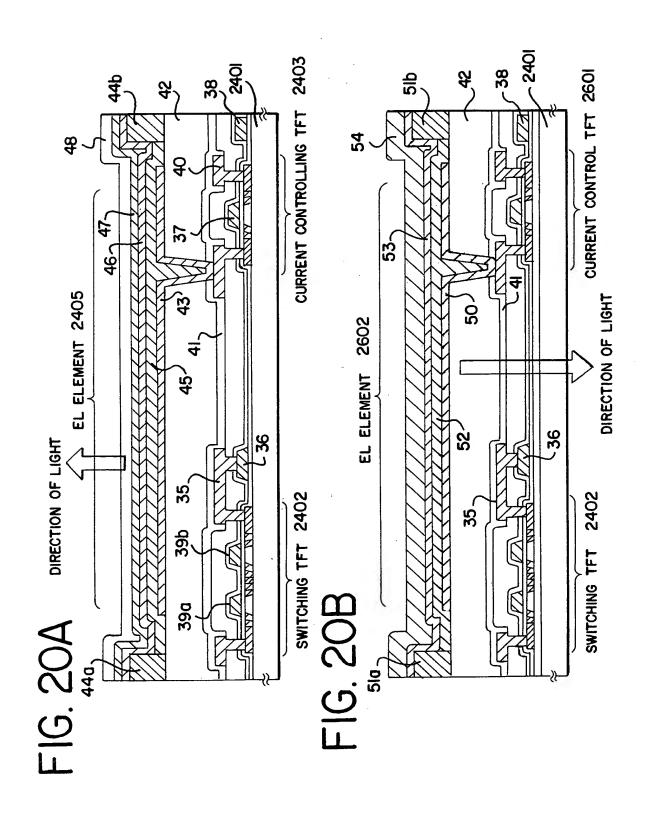


FIG. 17







## FIG. 2IA

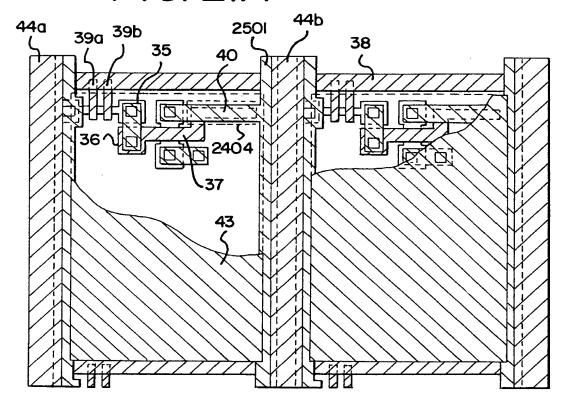


FIG. 2IB

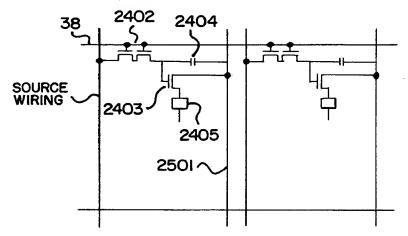


FIG. 22A

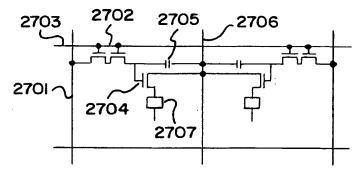


FIG. 22B

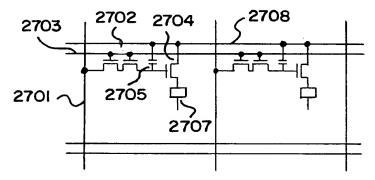


FIG. 22C

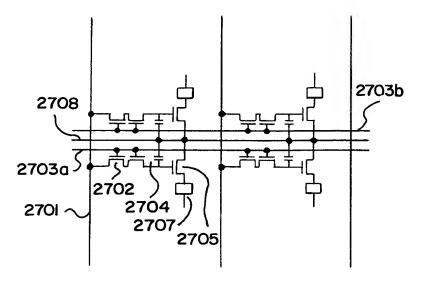


FIG. 23A

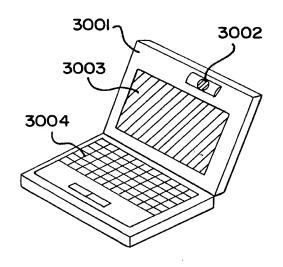


FIG. 23B

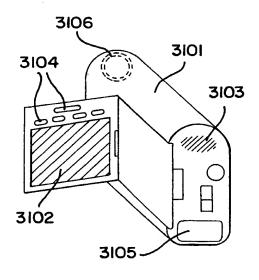


FIG. 23C

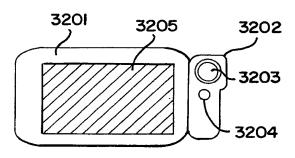


FIG. 23D



FIG. 23E

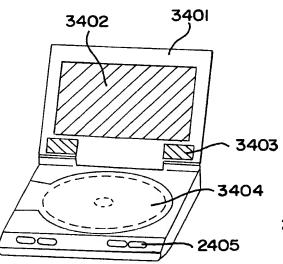


FIG. 23F

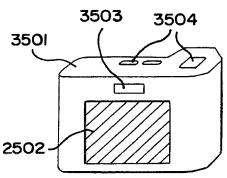
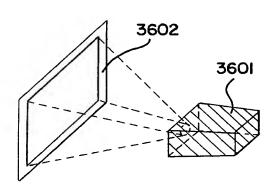


FIG. 24A

FIG. 24B



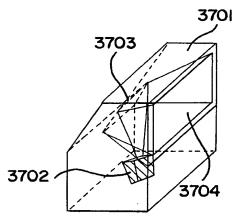


FIG. 24C

PROJECTION DEVICE (THREE PLATE TYPE)

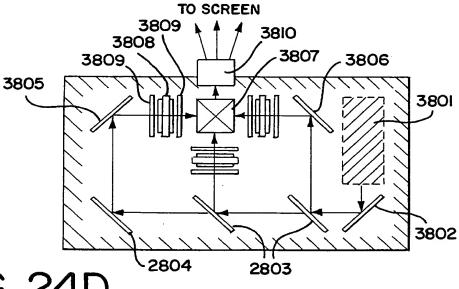
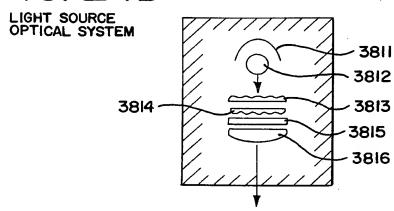
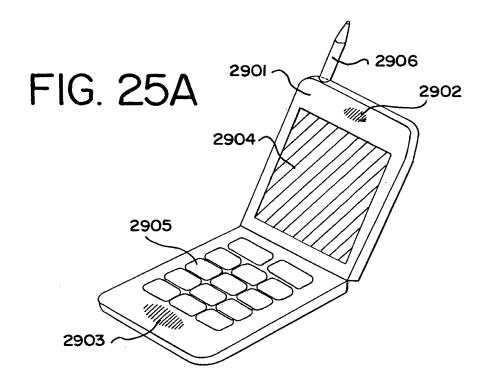
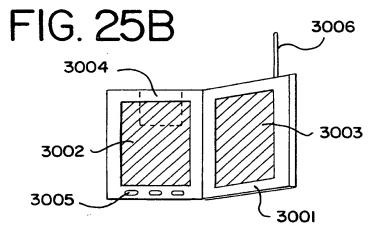
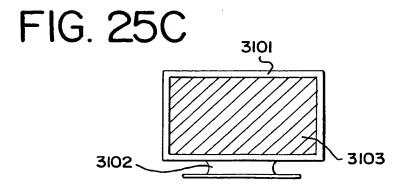


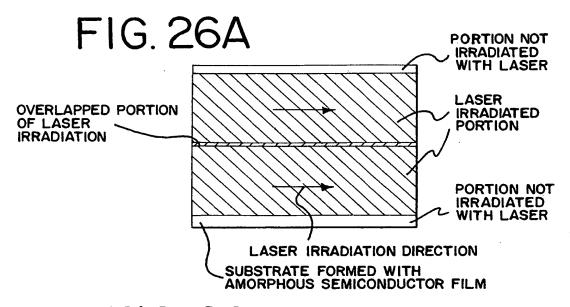
FIG. 24D











### FIG. 26B

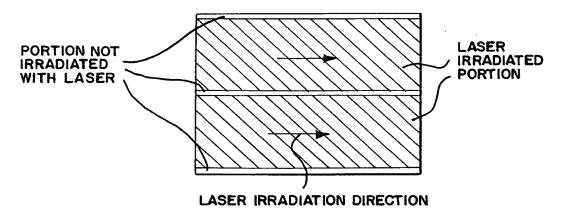


FIG. 26C

